



N-Channel Depletion-Mode Vertical DMOS FETs

Features

- ▶ High input impedance
- ▶ Low input capacitance
- ▶ Fast switching speeds
- ▶ Low on resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage

Applications

- ▶ Normally-on switches
- ▶ Solid state relays
- ▶ Converters
- ▶ Constant current sources
- ▶ Power supply circuits
- ▶ Telecom

General Description

The Supertex DN3525 is a low threshold depletion-mode (normally-on) transistor utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Product marking for TO-243AA:
DN5C*
 where * = 2-week alpha date code

Ordering Information

| BV _{DSX} / BV _{DGX} | R _{DS(ON)} (max) | I _{DSS} (min) | Package Options |
|--|------------------------------|---------------------------|-----------------------|
| | | | TO-243AA ¹ |
| 250V | 6.0Ω | 300mA | DN3525N8 |
| | | | DN3525N8-G |

-G indicates package is RoHS compliant ('Green')
Notes: ¹Same as SOT-89.



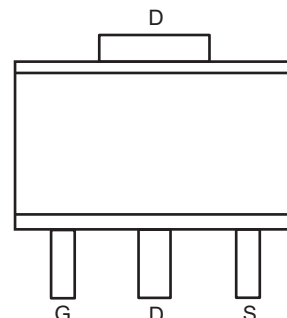
Absolute Maximum Ratings

| Parameter | Value |
|-----------------------------------|-------------------|
| Drain-to-source voltage | BV _{DSX} |
| Drain-to-gate voltage | BV _{DGX} |
| Gate-to-source voltage | ±20V |
| Operating and storage temperature | -55°C to +150°C |
| Soldering temperature* | 300°C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

*Distance of 1.6mm from case for 10 seconds.

Pin Configuration



TO-243AA
(top view)

Thermal Characteristics

| Package | I_D (continuous) ¹ | I_D (pulsed) | Power Dissipation @ $T_A = 25^\circ\text{C}$ | θ_{jc} ($^\circ\text{C/W}$) | θ_{ja} ($^\circ\text{C/W}$) | I_{DR}^1 | I_{DRM} |
|----------|------------------------------------|-------------------|---|--------------------------------------|--------------------------------------|------------|-----------|
| TO-243AA | 360mA | 1.0A | 1.6W ² | 15 | 78 ² | 360mA | 1.0A |

Notes:

- I_D (continuous) is limited by max rated T_J .
- Mounted on FR4 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

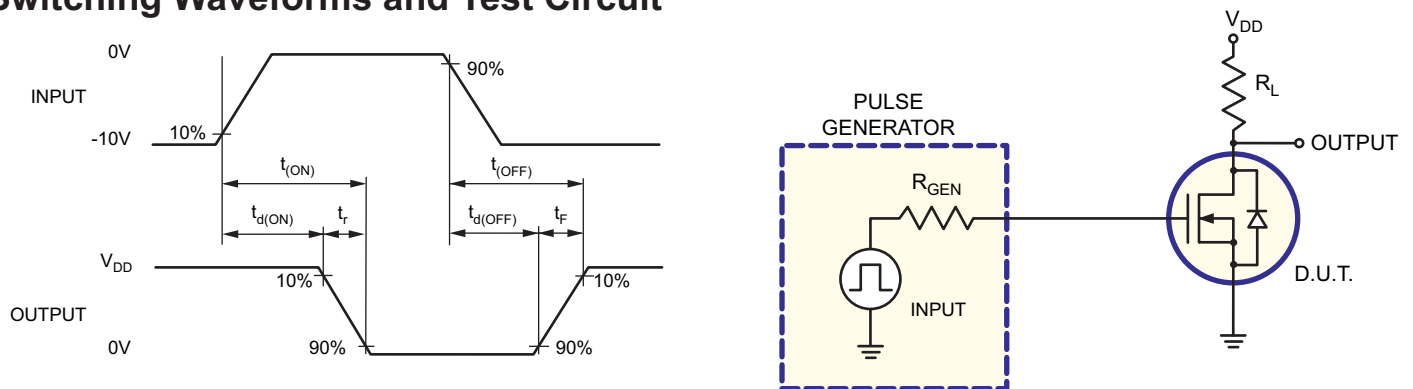
Electrical Characteristics (@25°C unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------------------|--|------|-----|------|----------------------|---|
| BV_{DSX} | Drain-to-source breakdown voltage | 250 | - | - | V | $V_{GS} = -5.0\text{V}, I_D = 100\mu\text{A}$ |
| $V_{GS(OFF)}$ | Gate-to-source OFF voltage | -1.5 | - | -3.5 | V | $V_{DS} = 15\text{V}, I_D = 1.0\text{mA}$ |
| $\Delta V_{GS(OFF)}$ | Change in $V_{GS(OFF)}$ with temperature | - | - | 4.5 | mV/ $^\circ\text{C}$ | $V_{DS} = 15\text{V}, I_D = 1.0\text{mA}$ |
| I_{GSS} | Gate body leakage current | - | - | 100 | nA | $V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$ |
| $I_{D(OFF)}$ | Drain-to-source leakage current | - | - | 1.0 | μA | $V_{DS} = \text{Max rating}, V_{GS} = -5.0\text{V}$ |
| | | - | - | 1.0 | mA | $V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = -5.0\text{V}, T_A = 125^\circ\text{C}$ |
| I_{DSS} | Saturated drain-to-source current | 300 | - | - | mA | $V_{GS} = 0\text{V}, V_{DS} = 15\text{V}$ |
| $R_{DS(ON)}$ | Static drain-to-source ON-state resistance | - | - | 6.0 | Ω | $V_{GS} = 0\text{V}, I_D = 200\text{mA}$ |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with temperature | - | - | 1.1 | %/ $^\circ\text{C}$ | $V_{GS} = 0\text{V}, I_D = 200\text{mA}$ |
| G_{FS} | Forward transconductance | 225 | - | - | mmho | $V_{DS} = 10\text{V}, I_D = 150\text{mA}$ |
| C_{ISS} | Input capacitance | - | 270 | 350 | pF | $V_{GS} = -5.0\text{V}, V_{DS} = 25\text{V}, f = 1.0\text{MHz}$ |
| C_{OSS} | Common source output capacitance | - | 20 | 60 | | |
| C_{RSS} | Reverse transfer capacitance | - | 5.0 | 20 | | |
| $t_{d(ON)}$ | Turn-ON delay time | - | - | 20 | ns | $V_{DD} = 25\text{V}, I_D = 150\text{mA}, R_{GEN} = 25\Omega, V_{GS} = 0\text{V to } -10\text{V}$ |
| t_r | Rise time | - | - | 25 | | |
| $t_{d(OFF)}$ | Turn-OFF delay time | - | - | 25 | | |
| t_f | Fall time | - | - | 40 | | |
| V_{SD} | Diode forward voltage drop | - | - | 1.8 | V | $V_{GS} = -5.0\text{V}, I_{SD} = 150\text{mA}$ |
| t_{rr} | Reverse recovery time | - | 800 | - | ns | $V_{GS} = -5.0\text{V}, I_{SD} = 150\text{mA}$ |

Notes:

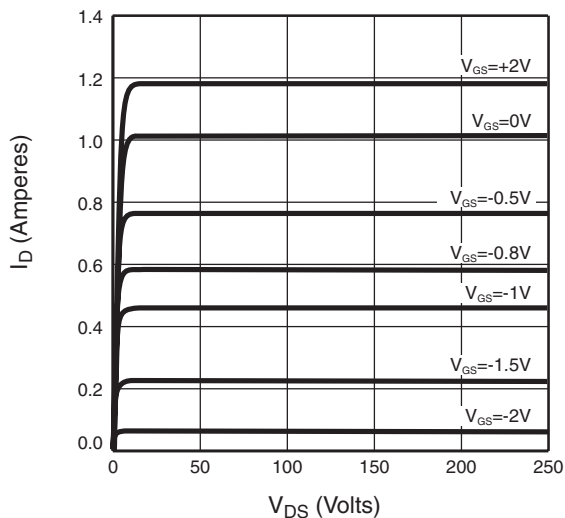
- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

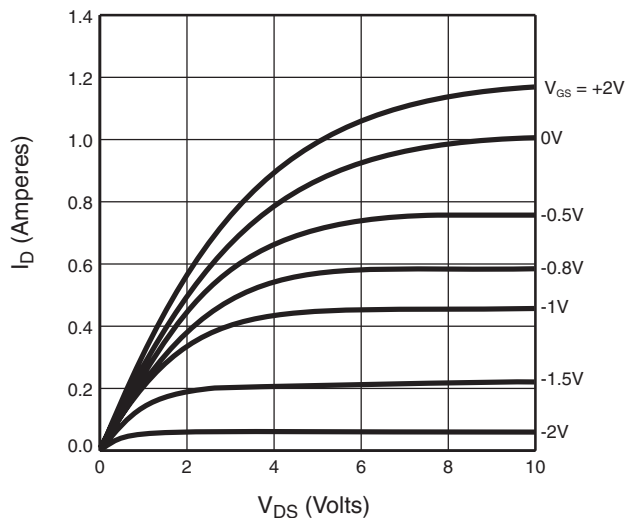


Typical Performance Curves

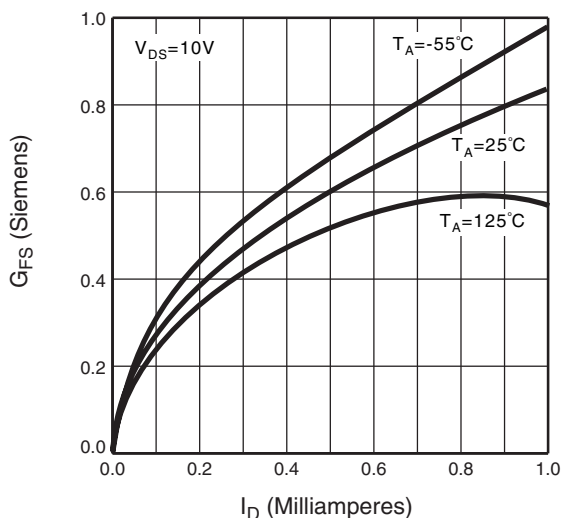
Output Characteristics



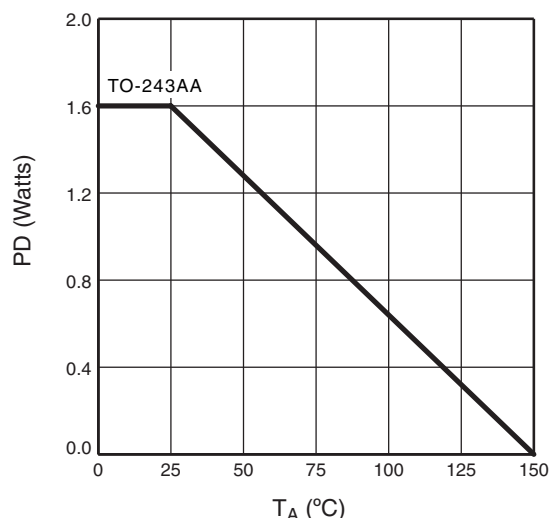
Saturation Characteristics



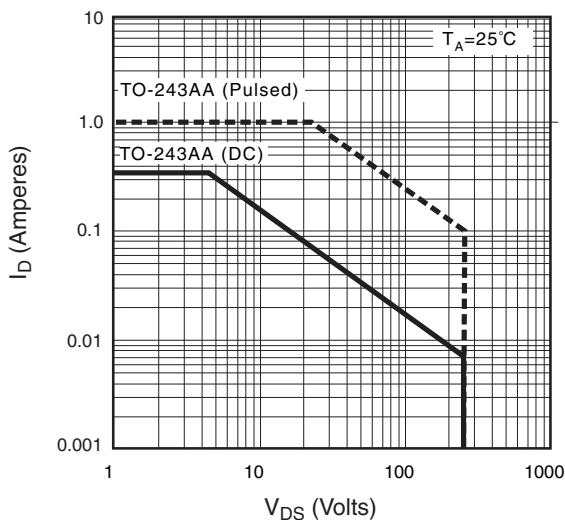
Transconductance vs. Drain Current



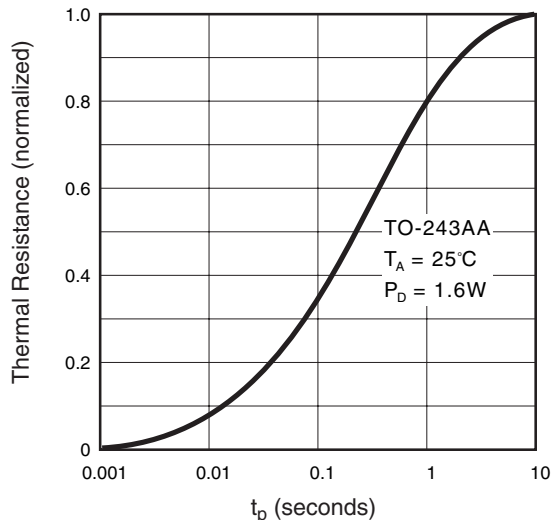
Power Dissipation vs. Ambient Temperature



Maximum Rated Safe Operating Area

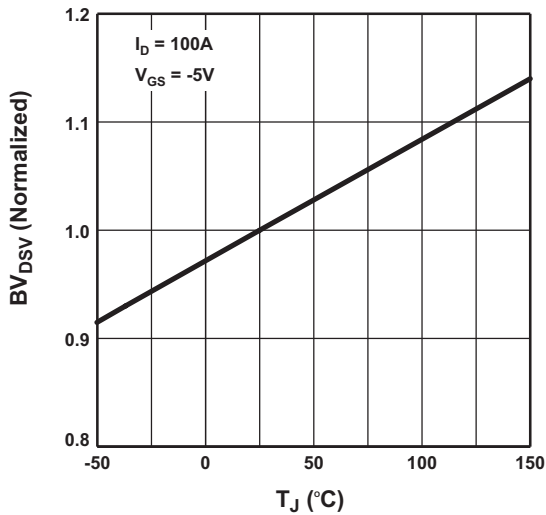


Thermal Response Characteristics

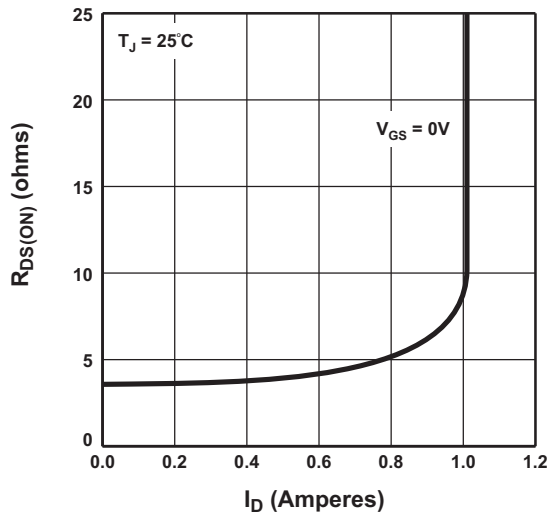


Typical Performance Curves (cont.)

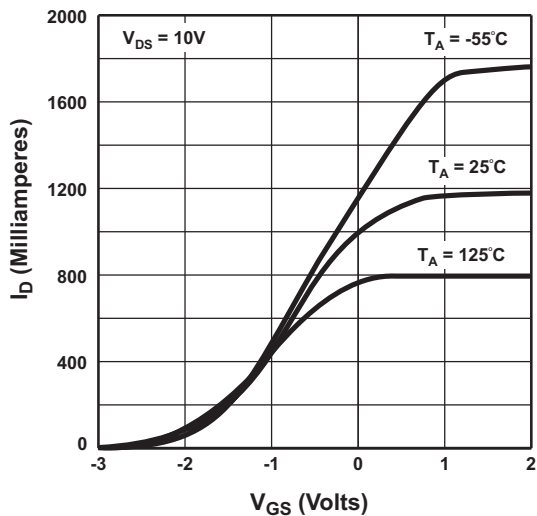
BV_{DSV} Variation with Temperature



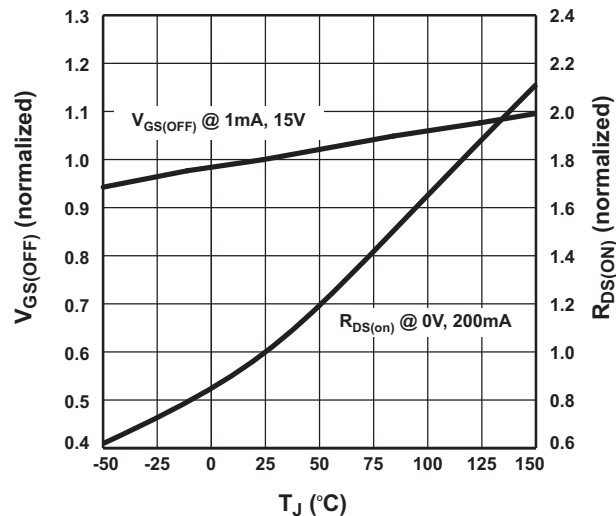
On Resistance vs. Drain Current



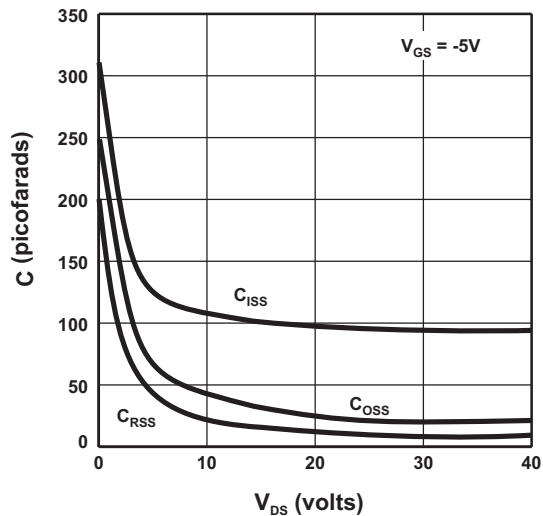
Transfer Characteristics



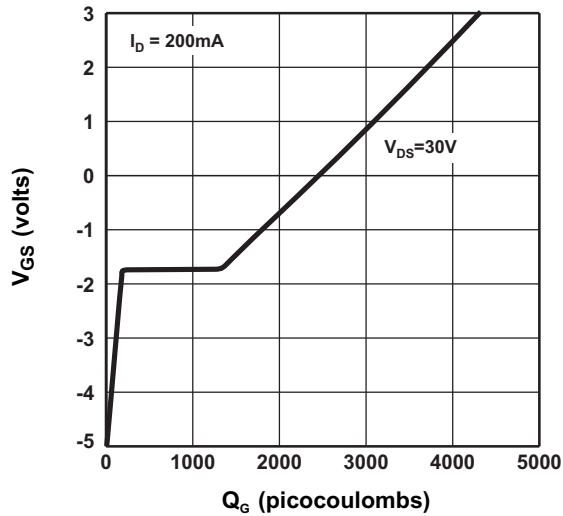
V_{GS(OFF)} and R_{DS(ON)} w/ Temperature



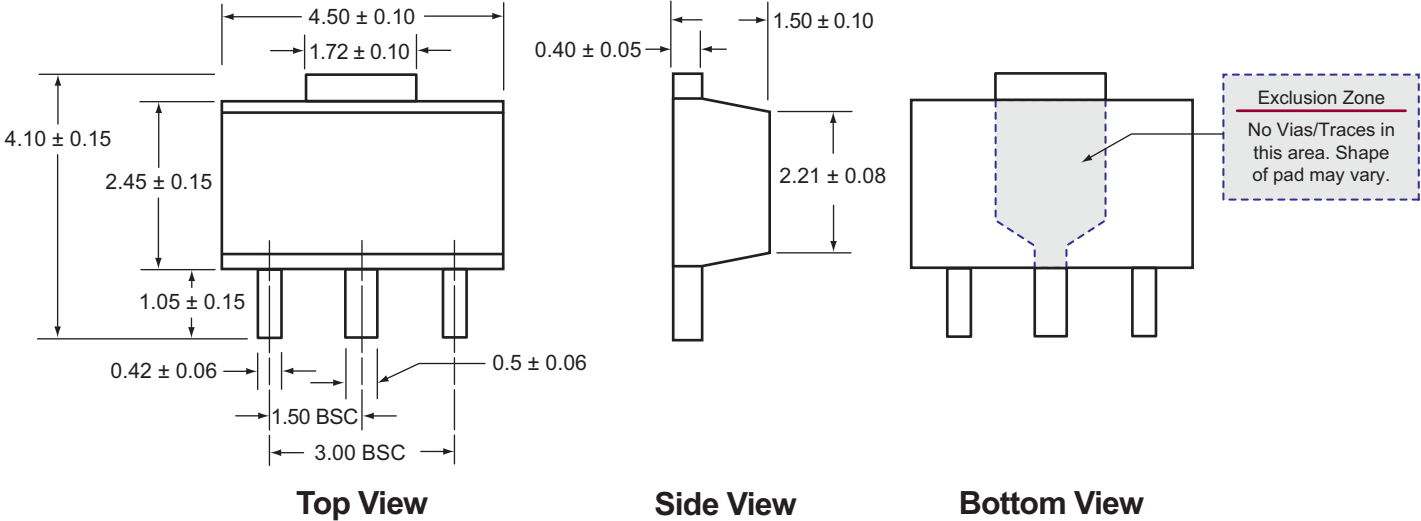
Capacitance vs. Drain Source Voltage



Gate Drive Dynamic Characteristics



3-Lead TO-243AA (SOT-89) Surface Mount Package (N8)



Notes:
All dimensions are in millimeters; all angles in degrees.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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